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(54) Semiconductor device.

(57) An N-InP buffer layer (22) is deposited on an N^+-InP substrate (21), an InGaAs light-absorbing layer (23) is deposited on the buffer layer (22), an N^--InP cap layer (24) is deposited on the light-absorbing layer (23), and a P-type impurity region (25) is formed in the light-absorbing layer (23) and the cap layer (24). Next, a masking film is formed on the cap layer (24), and with this masking film serving as a mask, the cap layer (24), the light-absorbing layer (23), the buffer layer (22) are etched, thus forming a P-type electrode forming region (27) and an N-type electrode forming region (28). Next, an insulating film (29) is provided for the periphery portion of the P-type impurity region (25) of the cap layer (24). Electrode pads (33) and (34) having a laminated structure are formed respectively on the P-type and N-type electrode forming regions (27) and (28), and a non-metal member (35) is formed on the insulating film (29) and on the surface, the periphery and the side surface of the electrode pad (33) of the P-type electrode.

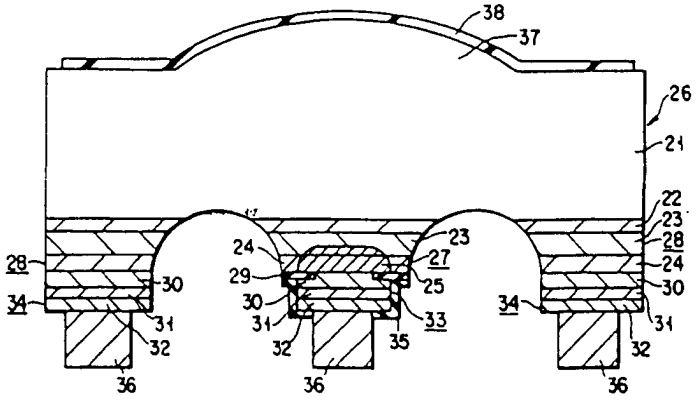

FIG. 4

EP 0 660 403 A1

The present invention relates to a compound semiconductor device, more specifically to an electrode structure capable of preventing deterioration of a semiconductor caused by a particular type of metal reacting there with, and enhancing the strength of mounting a metal electrode on a certain section so as to prevent the metal electrode from falling off, thereby increasing the reliability of the device, and simplifying the manufacturing process.

Generally, an electronic device such as a transistor or a diode, in which a compound semiconductor is used, or a compound semiconductor device such as an optical device including a laser diode or photodiode, has a metal electrode designed for the connection with an external electric circuit. Conventionally, the connection between a metal electrode and an external electric circuit is carried out in the following manner. That is, with regard to one of the electrodes, a compound semiconductor chip is mounted on a wiring pattern of a substrate, whereas with regard to the other electrode, a wire of Au, Al or the like is bonded. In this connecting method, a wire must be bonded, and therefore the manufacturing process becomes complex. The addition of the wire causes an increase in the electric capacity or inductance. Therefore, with the conventional method, it is difficult to obtain the electrical performances which the compound semiconductor originally possesses.

As a solution to this problem, recently, a so-called flip-chip type structure, capable of achieving the electrical connection by simply mounting a compound semiconductor device. The following is a description of the compound semiconductor device, taking an example of the electrode structure in a semiconductor light-receiving element for optical communications.

FIG. 1 is a cross section showing a conventional semiconductor light-receiving element of a flip-chip type, in which light is made incident from the rear surface. The light-receiving element 6 consists of an N^+-Inp substrate 1, an N-InP buffer layer 2, an InGaAs light absorption layer 3 and an N^--InP cap layer 4.

More specifically, first, the N-InP buffer layer 2 is provided on the N^+-InP substrate 1, and the InGaAs light absorption layer 3 is provided on the N-InP buffer layer 2. Then, the N^--InP cap layer 4 is formed on the InGaAs light absorption layer 3.

After that, for example, Zn is implanted selectively into the cap layer 4 as a P-type impurity, and a P-type impurity region 5 is formed in the light absorption layer 3 and the cap layer 4. Thus, a PN junction is formed between the P-type impurity region 5 and the light absorbing layer 3. Next, the cap layer 4, the light receiving layer 3 and the buffer layer 2 are etched, and these layers 4, 3 and 2 are separated into a region 7 in which a P-type electrode is formed (P-type electrode formation region) and a region 8 in which an N-type electrode is formed (N-type electrode formation region).

An insulating film 9 is provided on the cap layer 4 in the P-type electrode formation region 7. After that, a contact hole 9a is formed in the insulating film 9 at a location above the P-type impurity region 5. Next, a first electrode pad 13, which consists of a Ti layer 10, a Pt layer 11 and an Au layer 12, is provided in the contact hole 9a and on the insulating film 9, and a second electrode pad 14, which consists of the Ti layer 10, the Pt layer 11 and the Au layer 12, is provided on the cap layer 4 of the N-type electrode formation region 8.

After that, solder bumps (not shown) are formed on the first and second electrode pads 13 and 14. Next, a lens 15 is formed on the rear surface side of the N^+-InP substrate 1, on which light is made incident. A reflection preventing film 16 is formed on the lens 15.

FIG. 2 is a cross section showing an enlarged view of the main portion of the peripheral portion of the electrode obtained when the semiconductor light-receiving element shown in FIG. 1 is mounted on a mounting member. The flip-chip type semiconductor light receiving element, to which light is applied from the rear surface, is mounted on the mounting member 18 on which an electrode pattern 19 which corresponds to each of the electrode pads 13 and 14 is formed in advance with solder bumps 17 by the thermal pressure adhesion method.

The semiconductor light receiving element does not require a wire for wiring, and therefore the manufacture process can be simplified, and decreases in electric capacity and inductance can be suppressed. For the above-described reason, the above-described light receiving element has become the main focus of studies relating to the field of large capacity light receiving system, the demand of which has recently increased in recent times.

In the conventional rear-surface light incident flip-chip type semiconductor light receiving element, a possible pattern for the electrode pattern 19 is restricted, and therefore the area of the joint of the Ti layer 10, and the electrode forming regions 7 and 8 is rendered small as compared to the area of the chip surface. As a result, a stress is concentrated on the joint of the Ti layer 10, and the electrode forming regions 7 and 8 after the semiconductor light-receiving element is mounted on the mounting member 18, and therefore the semiconductor light receiving element, in some cases, fall off from the joint. In short, in the conventional semiconductor light-receiving element, a sufficient junction strength, which is required for preventing

ted on the mounting member;

FIG. 3 is a cross section schematically showing a region eroded by a solder component, in the periphery of the electrode when the flip-chip type semiconductor light-receiving element shown in FIG. 1 is mounted on the mounting member;

FIG. 4 is a cross section showing a flip-chip type semiconductor light-receiving element in which light is made incident from the rear surface thereof, according to the first embodiment of the present invention; and

FIG. 5 is a cross section showing a flip-chip type semiconductor light-receiving element in which light is made incident from the rear surface thereof, according to the second embodiment of the present invention.

Embodiment of the present invention will now be described in detail with reference to drawings.

FIG. 4 is a cross section showing a flip-chip type semiconductor light-receiving element in which light is made incident from the rear surface thereof, according to the first embodiment of the present invention. A light-receiving element 26 consists of an N^+-InP substrate 21, an N-InP buffer layer 22, an InGaAs light-absorbing layer 23 and an N^--InP cap layer 24.

More specifically, first, the N-InP buffer layer 22 having a carrier concentration of 1×10^{15} cm^{-3} and a thickness of 2 μm is deposited on the surface of the N^+-InP substrate 21 by MOCVD (metal organic chemical vapor deposition) method. Then, the InGaAs light absorbing layer 23 having a thickness of 2 μm is deposited on the N-InP buffer layer 22 by the MOCVD method. Next, the N^--InP cap layer 24 having a carrier concentration of 1×10^{15} cm^{-3} and a thickness of 1 μm is deposited on the InGaAs light-absorbing layer 23 by the MOCVD method.

After that, the first silicon nitride film (not shown) is deposited on the cap layer 24 by plasma CVD method. The first silicon nitride film is patterned by photolithography, and thus the first mask film (not shown) made of silicon nitride is formed on the cap layer 24. Next, the InP substrate 21 is placed in a diffusion furnace (not shown). Next, in an atmosphere of zinc dimethyl gas, under the conditions that the temperature is set to 500°C and the time period is set to 30 minutes, zinc is selectively diffused into the light-absorbing layer 23 and the cap layer 24, using the first masking film as a mask. Thus, a P-type impurity region 25 is formed in the light-absorbing layer 23 and the cap layer 24. Consequently, a PN junction is formed between the light-absorbing layer 23 and the P-type impurity region 25.

Next, the first masking film is removed. After that, the second silicon nitride film (not shown) is deposited on the cap layer 24. The second silicon nitride film is patterned by photolithography, and thus the second masking film (not shown) made of silicon nitride is formed on the cap layer 24. With using of the second masking film as a mask, the cap layer 24, the light absorbing layer 23 and the buffer layer 22 are removed by wet etching. Next, the second masking film is removed, and a region 27 in which a P-type electrode consisting of the cap layer 24, the light-absorbing layer 23 and the buffer layer 22 is formed (P-type electrode forming region), and regions 28 in each of which an N-type electrode is formed (N-type electrode forming region) are formed. The P-type electrode forming region 27 is situated between the N-type electrode forming regions 28.

After that, an insulating film 29 made of, for example, a silicon nitride film, is provided on the periphery portion of the P-type impurity region 25 on the surface of the cap layer 24. Next, a first electrode pad 33 having a multilayer structure is formed on the P-type electrode forming region 27, and a second electrode pad 34 having a multilayer structure is formed on each of the N-type electrode forming region 28, both by the vacuum deposition method. More specifically, a Ti layer 30 having a thickness of 100 nm is formed on the P-type electrode forming region 27, the P-type impurity region 25 and the insulating film 29 by the vacuum deposition method, and a Pt layer 31 having a thickness of 100 nm is formed on the Ti layer 30 by the vacuum deposition method. Further, an Au layer 32 having a thickness of 100 nm is formed on the Pt layer 31 by the vacuum deposition method. Thus, the first electrode pad 33 consisting of the Ti layer 30, the Pt layer 31 and the Au layer 32 is formed on the P-type impurity region 25 and the insulating film 29, and the second electrode pads 34 each consisting of the Ti layer 30, the Pt layer 31 and the Au layer 32 are formed on the cap layers 24.

The insulating film 29 serves to electrically insulate the first electrode pad 33 and the N^--InP cap layer 24 from each other. The Ti layer 30 functions as a contact layer for assuring the electrical contact with the InP cap layer 24 in each of the P-type electrode forming region 27 and the N-type electrode forming regions 28. The Pt layer 31 functions as a barrier layer for preventing the mutual diffusion of metal elements between the Ti layer 30 and the Au layer 32. The Au layer 32 is integrated with the solder bumps after the mounting step so as to achieve the electrical junction.

Next, a non-metal member 35 made of a silicon nitride film, is deposited on the first and second electrode pads 33 and 34 and the insulating film 29 by the plasma CVD method. After that, the non-metal member 35 is patterned by the photolithography, and thus the non-metal member 35

the falling-off of the device, cannot be obtained. As a solution to this problem, it may be considered that the area of the junction should be increased; however when the area of the junction is increased, the area of the PN junction is inevitably increased. With this increment, the electric capacity in the PN junction is increased, resulting in degradation of the performances of the semiconductor light receiving element.

Further, as shown in FIG. 2, the solder bumps 17 are melted on the electrode pad 13 and flows on the side surface of the electrode pad 13 in the mounting step. Consequently, a component such as Au or Sn, contained in the solder bumps 17 which have remained on the side surface, is not blocked by the Pt layer 11, which was supposed to serve as a barrier layer and prevent such entering of the solder components. Therefore, as shown in FIG. 3, the component flows onto the Ti layer 10, which is a contact layer, or underneath the layer. As a result, the component such as Au or Sn is diffused in the cap layer 4, which is a compound semiconductor region, and a region 20, which is made as the solder component erodes the cap layer 4, is formed. Due to the diffusion of Au or Sn, the PN junction of the semiconductor is destroyed, and the electrical or optical characteristics of the semiconductor element are degraded. The destruction of the junction may occur in the process of the mounting step; however it gradually proceeds when the compound semiconductor device obtained after the mounting process is used in practice. This results in a low long-term reliability of the device, which is particularly a serious problem in the case of the large-capacity optical communication system, for example.

In order to solve such a problem, the following idea has been proposed. That is, for example, the distance L from the contact hole 9a to the end of the first electrode pad 13 shown in FIG. 3 is increased so as to make the component Au or Sn not easily entering into the contact hole 9a. As the first technique, it is a possibility that the distance L is increased by expanding the first electrode pad 13 by the periphery thereof. With this expansion, the periphery of the P-type impurity region 5 expands outwards along the periphery of the first electrode pad 13. Consequently, the area of the PN junction of the P-type impurity region 5 increases to a certain degree; however it cannot be increased to a sufficient level due to the restrictions of electrical capacity. Therefore, the first technique is not very appropriate. As the second method, it is a possibility that the distance L is increased by reducing the size of the contact hole 9a of the insulating film 9. In this case, the contact area between the first electrode pad 13 and the electrode forming region 7 is made small; however it is not desired to reduce the size of the contact area very much because of the restriction of the contact resistance. In practice, it is difficult to increase the distance L to a sufficient level. Thus, with the conventional technique, the problem of a low long-term reliability cannot be solved.

The object of the present invention is to provide a semiconductor device having a high reliability and a high contact strength of the element after the element is mounted on the mount member.

The object can be achieved by a semiconductor device comprising:

a semiconductor chip having a structure in which an electrode is provided on a semiconductor substrate;

an electrode pad provided on the electrode;

a non-metal member provided for a surface, a periphery and a side surface of the electrode pad; and

a mounting member for mounting the semiconductor chip with solder, by using an upper surface of the electrode pad as a contact surface.

According to the present invention, a non-metal member is provided for the surface, periphery and side surface of the electrode pad. With the member, the overflowing of the melted solder to the side surface of the electrode pad and the side surface of the electrode, which may take place when the semiconductor chip is mounted on the mounting member, can be prevented. With this structure, a component contained in solder does not overflow underneath the electrode pad, and therefore the deterioration of the electrical or optical characteristics of the semiconductor chip can be prevented. Thus, the reliability of the semiconductor device is not deteriorated.

Further, with the non-metal member provided for the surface, periphery and side surface of the electrode pad, the electrode pad is firmly fixed to the electrode. The electron pad can stand the tensile stress or dicing stress very remarkably as compared to the conventional semiconductor device, in which no non-metal member is provided. Thus, the strength of preventing the falling-off of the semiconductor chip can be very much enhanced.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a cross section showing a conventional flip-chip type semiconductor light-receiving element in which light is made incident from the rear surface thereof;

FIG. 2 is a cross section showing an enlarged view of the main portion of the periphery of the electrode when the flip-chip type semiconductor light-receiving element shown in FIG. 1 is moun-

According to the results of an accelerated degradation test carried out at an applied bias of 20V and at a temperature of 250 °C, the average life of the conventional flip-chip type semiconductor light receiving element is 1000 hours or less, whereas the average life of the semiconductor light receiving device of 2000 hours or more. It was confirmed from the results that the life of the element could be drastically prolonged. The reason for being able to prolong the life of element is that the non-metal member 35 which covers the first electrode pad 33, serves as a protection layer for the electrode forming region 27, thus avoiding the entering and diffusion of a solder component element from the side surface of the first electrode pad 33.

Since the non-metal member 35 is provided for the side surface and the like of the first electrode pad 33, the non-metal member 35 can be used as a mask when the solder bump 36 is formed on the first electrode pad 33 by the electrolytic plating method. Therefore, the solder bump 36 can be easily formed at a desired position with accuracy, and thus the manufacturing process can be facilitated, and the production cost can be reduced.

The first embodiment is described in connection with the case where the present invention is applied to a flip-chip type semiconductor light receiving element to which light is made incident from the rear surface; however the present invention is can be applied to other semiconductor devices, for example, electronic devices such as a light-emitting diode, a semiconductor laser, a high mobility transistor (HEMT), an electric field effect transistor (MISFET or MOSFET) and a hetero bipolar transistor (HBT), or an optoelectronic IC obtained by combining these devices.

In the above embodiment, the present invention is applied to an InP or InGaAs compound semiconductor device; however the invention can be applied to other compound semiconductor devices, for example, GaAs, AlGaAs, ZnSe or CdTe compound semiconductor devices.

In this embodiment, the non-metal member 35 made of silicon nitride is deposited on the first and second electrode pads 33 and 34; however it is also a possibility that a non-metal member made of silicon oxide or polyimide, is deposited on the first and second electrode pads 33 and 34.

In this embodiment, the electrode pads 33 and 34 having a three-layer structure made of the Ti layer 30, the Pt layer 31 and the Au layer 32, are formed respectively on the first and second electrode pads 33 and 34; however it is also a possibility that electrode pads having a metal layer made of one element selected from the group consisting of at least Ni, Pd, Pt, Rh and Ti are formed respectively on the P-type electrode forming region 27 and the N-type electrode forming regions 28.

In this embodiment, the electrode pads 33 and 34 having a laminated-layer structure are formed respectively on the P-type electrode forming region 27 and the N-type electrode forming regions 28; however it is also a possibility that electrode pads made of a single metal layer are formed respectively on the P-type electrode forming region 27 and the N-type electrode forming regions 28.

In this embodiment, the solder bump 36 containing Au and Sn is formed on each of the first and second electrode pads 33 and 34; however it is also a possibility that solder bumps mainly containing one element selected from the group consisting of at least Au, Sn, Pb and In are formed respectively on the first and second electrode pads 33 and 34.

FIG. 5 is a cross section showing a flip-chip type semiconductor light-receiving element in which light is made incident from the rear surface thereof, according to the second embodiment of the present invention, and the same structural elements as those shown in FIG. 4 are designated by the same reference numerals. With regard to the second embodiment, only sections different from those of the first embodiment will be described.

In the second embodiment, no solder bumps are formed on the first and second electrode pads 33 and 34, and therefore solder must be supplied in a so-called preform, when a semiconductor light-receiving element is mounted on a ceramic carrier (not shown) of an exclusive use. The preform of solder is a lump having a predetermined size. The solder mainly contains one of at least Au, Sn, Pb and In.

A preform lump of solder is placed on the ceramic carrier, and the solder is melted by heat. While the solder is in a molten state, the semiconductor light receiving element is mounted on the ceramic carrier, and the semiconductor light-receiving element is fixed by the solder.

In the second embodiment, the same advantage as that of the first embodiment can be achieved.

In the second embodiment, solder is supplied in preform when mounting an light-receiving element; however it is also a possibility that solder is formed in advance on the exclusive-use ceramic carrier.

Claims

1. A semiconductor device characterized by comprising:

   a semiconductor chip (26) having a structure in which an electrode (27, 28) is provided on a semiconductor substrate (21);

   an electrode pad (33, 34) provided on said electrode (27, 28); and

is formed on the insulating film 29 and the surface, the periphery and the side surface of the first electrode pad 33.

After that, a solder bump 36 made of Au and Sn is provided on each of the first and second electrode pads 33 and 34 by an electric plating method. Then, a lens-like resist (not shown) is formed on the rear surface, which is the light incident side, of the N^+-InP substrate 21. This resist and the entire rear surface of the N^+-InP substrate 21 are polished by ion milling, thus forming an InP monolithic lens 37 on the rear side of the InP substrate 21. Then, a reflection preventing film 38 made of silicon nitride is formed on the lens 37 and the rear surface of the InP substrate 21 by the plasma CVD method.

The flip-chip type semiconductor light receiving element, on which light is made incident from the rear surface, is mounted on the ceramic carrier (not shown) used only as a mounting member, by the solder bump 36 by thermal pressure adhesion method. Electrode patterns corresponding to the first and second electrode pads 33 and 34 are formed in advance on the surface of the ceramic carrier. Thus, the P-type electrode forming region 27 and the N-type electrode forming regions 28 are electrically connected to the ceramic carrier via the solder bump 36 and the first and second electrode pads 33 and 34.

In the first embodiment, the surface, the periphery and the side surface of the first electrode pad 33 is covered by the non-metal member 35. A melted portion of the solder bump 36, which results when the semiconductor light receiving element is mounted on the ceramic carrier by the thermal pressure method, can be prevented from coming around to the side surface of the first electrode pad 33. Consequently, the metal portion of the solder bump 36 can be prevented from changing properties of the semiconductor (see numeral 20 in FIG. 3), which is caused by diffusion of the metal portion into the semiconductor. Further, the melted portion of the solder bump 36 can be prevented from overflowing to the side surface of the P-type electrode forming region 27. More specifically, with the structure of the conventional flip-chip type semiconductor light receiving element, the melted portion of the solder bump overflows to the surface and the entire side surface of the electrode pad during the mounting step, and in some cases, even reaches the P-type electrode forming region by pressure adhesion. Such overflow of solder bump results in formation of excessive MIS (Metal-Insulator-Semiconductor) structure, causing an increase in electrical capacity and a decrease in ESD (Electro-Static-Discharge) threshold. In this embodiment, the side surface and the like of the electrode pad 33 is covered by the non-metal member 35, which suppress the diffusion of the melted portion of the solder bump 36, and therefore the melted portion does not overflow to the P-type electrode forming region 27. In other words, the non-metal member 35 has a low wettability with respect to solder, and therefore the melted portion of the solder bump 36 does not easily overspread. Thus, a melted portion of the solder bump 36 does not overflow to the side surface of the P-type electrode forming region 27. Consequently, a component contained in the solder bump 36, such as Au or Sn, does not diffuse to the Ti layer 30 or enter underneath the layer, and therefore the degradation of the electrical or optical characteristics of the semiconductor light receiving element can be avoided. Consequently, a decrease in the reliability of the compound semiconductor device can be prevented.

When a material having a particularly low wettability with respect to the solder bump 36 is selected as the material for the non-metal member 35, the above-described solder bump overflow suppressing effect can be further enhanced.

Moreover, when the first electrode pad 33 is covered by the non-metal member 35, the electrode pad 33 is firmly fixed to the P-type electrode forming region 27. Consequently, the first electrode pad 33 can be made remarkably strong against the tensile stress or dicing stress, as compared to the conventional compound semiconductor device in which the electrode pad is not covered by the non-metal member 35. Thus, the resistance to the falling-off of the element (to be called "adhesion strength" hereinafter) can be significantly improved. That is, even if the area of the contact surface between the Ti layer 30 of the first electrode pad 33 and the P-type electrode forming region 27 is small as compared to the size of the chip, the falling off of the semiconductor light receiving element from the mounting member, caused by the concentration of the stress to this joint, can be prevented. In other words, the falling off of the semiconductor light receiving element from the mounting member, can be prevented without increasing the area of the joint.

With regard to the conventional flip-chip type semiconductor light receiving element, the average adhesion strength of chips after being mounted is 30 gf, whereas with regard to the flip-chip type semiconductor light receiving element of the present invention, the average adhesion strength of chips after being mounted is 80 gf. Therefore, errors due to lack of the mounting strength, caused by falling-off of the electrode can be significantly suppressed. With the present invention, a series of original characteristics of the flip-chip type semiconductor light receiving element are as good as those of the conventional element.

a non-metal member (35) provided for a surface, a periphery and a side surface of said electrode pad (33, 34).

2. A semiconductor device characterized by comprising:
a semiconductor chip (26) having a structure in which an electrode (27, 28) is provided on a semiconductor substrate (21);
an electrode pad (33, 34) provided on said electrode (27, 28);
a non-metal member (35) provided for a surface, a periphery and a side surface of said electrode pad (33, 34); and
a solder bump (36) provided on a surface of said electrode.

3. A semiconductor device according to claim 2, characterized in that said solder bump (36) mainly contains one of the group consisting of at least Au, Sn, Pb and In.

4. A semiconductor device characterized by comprising:
a semiconductor chip (26) having a structure in which an electrode (27, 28) is provided on a semiconductor substrate (21);
an electrode pad (33, 34) provided on said electrode (27, 28);
a non-metal member (35) provided for a surface, a periphery and a side surface of said electrode pad (33, 34); and
a mounting member for mounting said semiconductor chip (26) with solder, by using an upper surface of said electrode pad (33, 34) as a contact surface.

5. A semiconductor device according to claim 1, 2 or 4, characterized in that said non-metal member (35) is made of silicon oxide, silicon nitride or polyimide.

6. A semiconductor device according to claim 2 or 5, characterized in that said electrode pad (33, 34) includes a metal layer made of at least Ni, Pd, Pt, Rh and Ti.

7. A semiconductor device according to claim 2 or 6, characterized in that said electrode pad (33, 34) is made of a single or a plurality of metal layers.

8. A semiconductor device according to claim 7, characterized in that said solder (36) mainly contains one of the group consisting of at least Au, Sn, Pb and In.

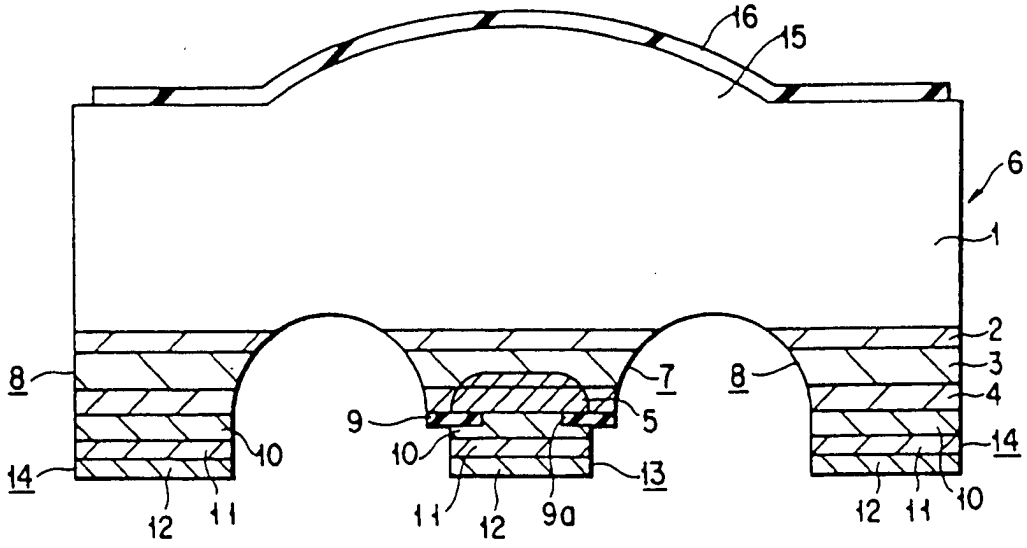

FIG. 1

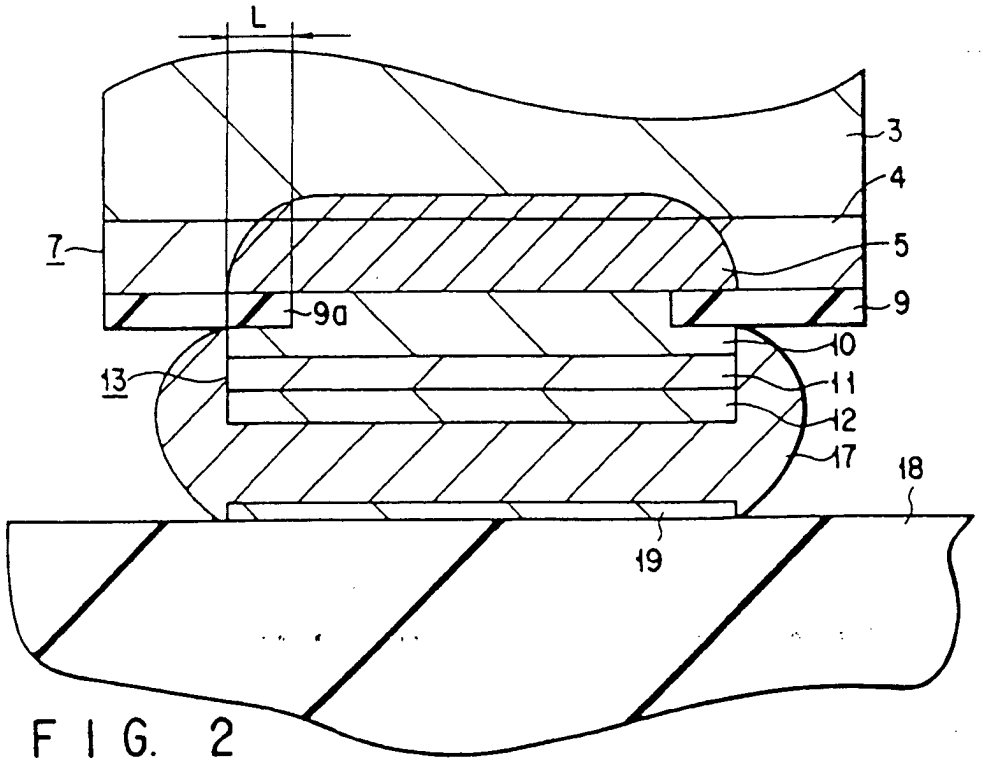

FIG. 2

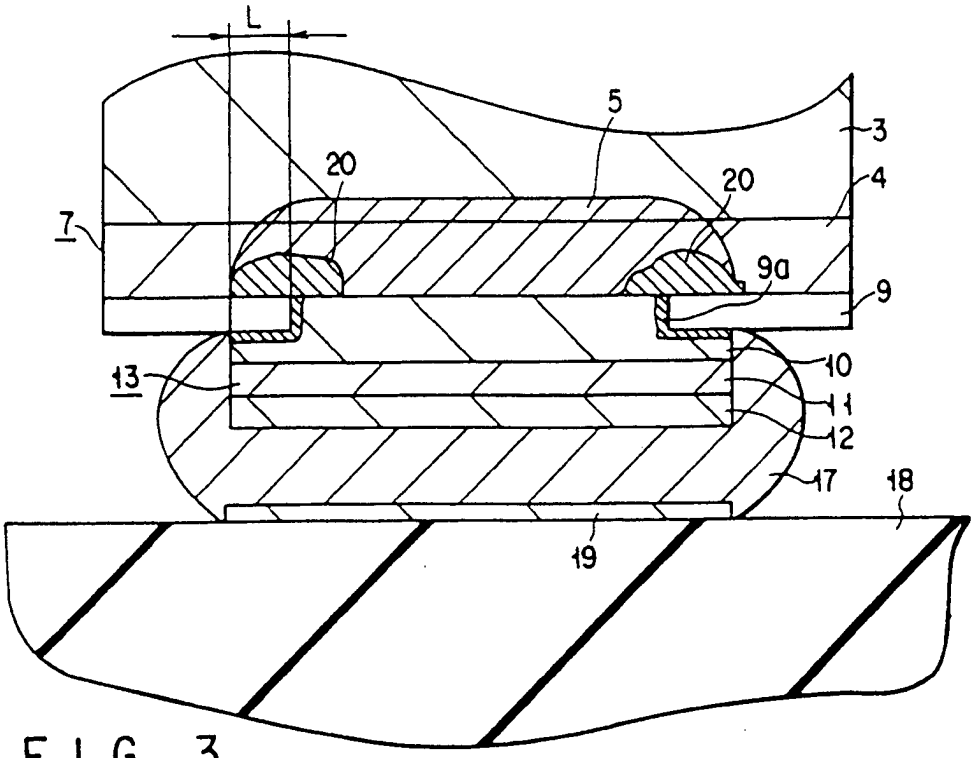
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FIG. 3

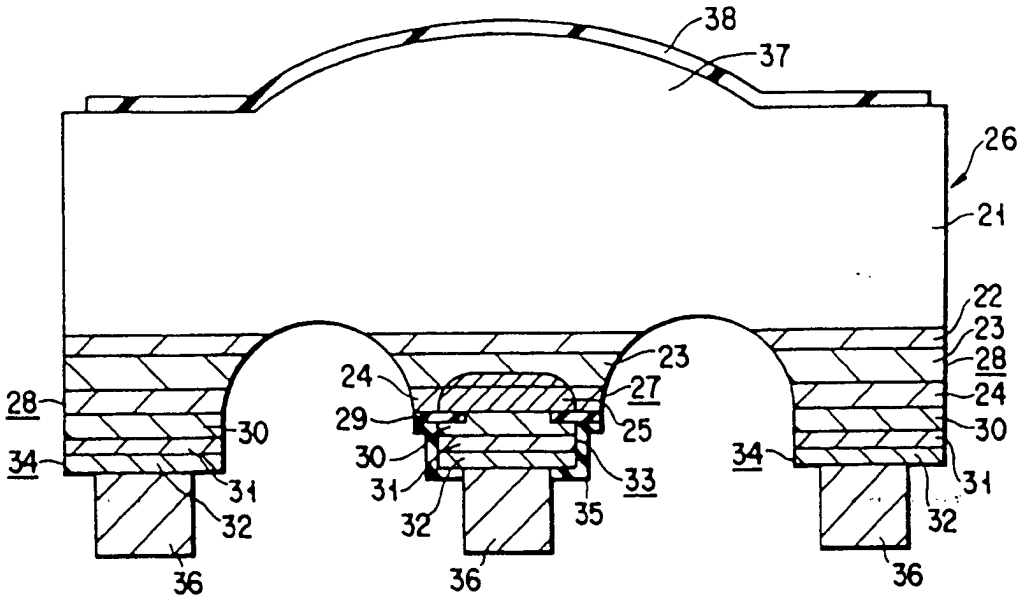
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FIG. 4

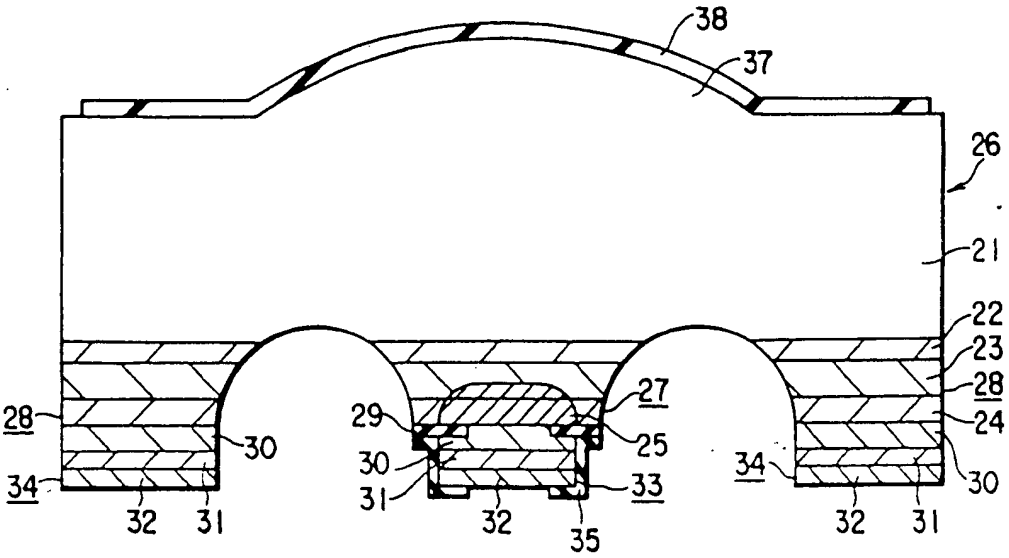
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FIG. 5

European Patent Office

PARTIAL EUROPEAN SEARCH REPORT

which under Rule 45 of the European Patent Convention shall be considered, for the purposes of subsequent proceedings, as the European search report

Application Number EP 94 12 0592

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US-A-3 716 907 (ANDERSON) * column 3, line 36 - column 4, line 31; figure 7 * ---	1,2,4	H01L23/485 H01L31/0224
A	US-A-4 258 382 (HARRIS) * column 2, line 58 - column 3, line 20 * ---	1	
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.27, no.9, February 1985, NEW YORK US page 5252 LEVINE ET AL 'solder terminal for semiconductor devices' * the whole document * ---	1-8	
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.20, no.12, May 1978, NEW YORK US page 5317 AHN ET AL 'Permalloy solder barrier for devices with gold conductor metallization' --- -/--	1-8	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

INCOMPLETE SEARCH

The Search Division considers that the present European patent application does not comply with the provisions of the European Patent Convention to such an extent that it is not possible to carry out a meaningful search into the state of the art on the basis of some of the claims

Claims searched completely :

Claims searched incompletely : 1-8

Claims not searched :

Reason for the limitation of the search:

see sheet C

Place of search	Date of completion of the search	Examiner
THE HAGUE	3 April 1995	Greene, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
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& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

PARTIAL EUROPEAN SEARCH REPORT

Application Number
EP 94 12 0592

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.36, no.10, October 1993, NEW YORK US pages 529 - 530 'solder bump formation with anti-erosion polyimide brim' * the whole document * ---	1-8	
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.21, no.3, August 1978, NEW YORK US page 1007 JADUS 'Flip chip terminal for semiconductor devises' * the whole document * ---	1-8	
A	IEEE PHOTONICS TECHNOLOGY LETTERS, vol.3, no.12, December 1991, NEW YORK US pages 1115 - 1116 KITO ET AL 'High-speed flip-chip InP/InGaAs avalanche photodiodes with ultralow capacitance and large gain-bandwidth products' * figure 1 * -----		TECHNICAL FIELDS SEARCHED (Int.Cl.6)

EPO FORM 1503 03.82 (P04C10)

(19) Europäisches Patentamt
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(11) Publication number: **0 588 040 A3**

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(54) Light source and technique for mounting light emitting diodes.

(57) A light emitting diode has both end faces metallized and is mounted on a substrate with the light emitting junction perpendicular to the substrate. The electrically conductive ends are electrically bonded to conductive areas on the substrate by solder or conductive adhesive. LED dice can be placed on the substrate by temporarily attaching the dice to a tape which has been wrapped around a knife edge. The dice tilt as the tape wraps around the edge and are picked off one at a time by a vacuum collet while temporarily supported by a movable finger, and then transferred by the vacuum collet to a substrate. A similar method may be used for placing semiconductor dice on a substrate without the tilting of dice around the edge. In another embodiment, an array of LEDs can be assembled in windows through a metallized plastic tape which is bonded to a foundation with additional metallized leads.

EP 0 588 040 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 11 2376

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	EP-A-0 303 272 (SIEMENS AKTIENGESELLSCHAFT BERLIN UND MÜNCHEN) * column 1, line 43 - column 2, line 13; figures 1,6 *	1,3,10, 11	H01L33/00
Y		1-3,10, 11,13,14	

X	PATENT ABSTRACTS OF JAPAN vol. 6, no. 123 (E-117)8 July 1982 & JP-A-57 049 284 (MATSUSHITA ELECTRIC IND CO LTD) 23 March 1982 * abstract *	13,14	
Y		1-3,10, 11,13,14	

A	PATENT ABSTRACTS OF JAPAN vol. 4, no. 32 (E-002)19 March 1980 & JP-A-55 003 690 (TOSHIBA CORP) 11 January 1980 * abstract *	1,2,5, 10,13	
	---		TECHNICAL FIELDS SEARCHED (Int.Cl.5)
A	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 32, no. 1 , June 1989 , NEW YORK US pages 459 - 461 'Placement head' * page 461, last paragraph; figure 1 *	15-17, 19,26,27	H01L H05K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 January 1994	De Laere, A

CATEGORY OF CITED DOCUMENTS

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L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EP 23 11 8276

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

See Sheet B.

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-14 : Light source whereby the light emitting diode is mounted on a substrate with the junction perpendicular to the substrate.

2. Claims 15-34 : Method for mounting a semiconductor dice on a substrate, whereby the die, attached on a flexible tape, is brought to the bent edge of the tape where it is removed from it.